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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,168	12/18/2001	Ralf Dorscheid	DE000234	5133

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EXAMINER	
REIS, TRAVIS M	
ART UNIT	**PAPER NUMBER**
2859	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,168	DORSCHEID ET AL.	
	Examiner	Art Unit	
	Travis M. Reis	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-8, & 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. (U.S. Patent 6292528) in view of Nakajyo et al. (U.S. Patent 6420213) & Yamamoto et al. (U.S. Patent 6265782).

Wieczorek et al. disclose a detector for the detection of electromagnetic radiation, i.e. X-rays (col. 3 line 10), of which said detector includes a scintillator (11), a CMOS chip (9), and a base element (15), wherein a respective intermediate layer (13) that is defined in respect of its gap width is arranged each time between the scintillator and the CMOS chip and a layer (16) between the CMOS chip and the basic element, wherein said intermediate layers contains an adhesive (13, 16), wherein said adhesive has some quantities applied to the surface of the scintillator that faces the CMOS chip as well as to bumps that are present on the CMOS chip while said adhesive also has some quantities (16) applied directly to the rear surfaces of the CMOS chip and the basic element.

Wieczorek et al. do not disclose the basic element is a ceramic element based on aluminum oxide. However, the particular type of material used to make the basic element, absent any criticality, is only considered to be the use of a " preferred " or " optimum " material out of a plurality of well known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation based, among other things, on the intended use of Applicant's apparatus,

i.e., suitability for the intended use of Applicant's apparatus, and since the courts have stated that a selection of a material on the basis of suitability for intended use of an apparatus would be entirely obvious. See In re Leshin, 125 USPQ 416 (CCPA 1960).

Wieczorek et al. do not disclose spacers.

Nakajyo et al. discloses a method for fixing a semiconductor device (1) having stud bumps/spacers (2) to a ceramic substrate (3) by an electrically non-conductive epoxy resin adhesive (7) (col. 6 lines 66-67 through col. 7 line 1), wherein the gap width is determined by the quantity of adhesive and a plurality of spacers (Figures 2 & 4). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to add the stud bumps/spacers disclosed by Nakajyo et al. to the adhesive layers & electric leads, i.e. the layer between the basic element and the CMOS chip; and the layer between the scintillator and the CMOS chip, disclosed by Wieczorek et al. in order to insure the standard flatness between the CMOS chip and bond pad, thereby minimizing the stretch between electrical leads by preventing one side edge to be higher than the other side edge.

Wieczorek does not disclose a second acrylate adhesive.

Yamamoto et al. discloses a semiconductor device, semiconductor chip mounting substrate, and method of manufacturing the device and substrate, adhesive, and adhesive double coated film using an adhesive comprised of the epoxy-group-containing acrylic copolymer adhesive and an additional epoxy resin used together in order to reduce the number of cracks and since it has an excellent reactivity with the epoxy resin and improves the adhesive film strength (col. 14 lines 46-64). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to add the epoxy-group-containing acrylic copolymer adhesive disclosed by Yamamoto et al. to the adhesive disclosed by Wieczorek in order to reduce the number of cracks and since it has an excellent

reactivity with the epoxy resin and improves the adhesive film strength.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al., Nakajyo et al., & Yamamoto et al. as applied to claims 1-4, 6-8, & 12-16 above, and further in view of Doyle et al. (U.S. Patent 6063688).

Wieczorek et al.,Nakajyo et al., & Yamamoto et al. disclose all of the instant claimed invention as stated above in the rejection of claims 1-4,6-8, & 12-16; including that the spacers can be made of Au, Al, and solder (Nakajyo et al. col. 7 lines 62-64).

Wieczorek et al.,Nakajyo et al., & Yamamoto et al. do not disclose the spacer is a wire.

Doyle et al. discloses the fabrication of deer submicron structures and quantum wire transistors using hard-mark transistor width definition, wherein quantum wires are used as spacers for the formation of gaps/trenches in the substrate surface (col. 7 lines 50 & 55-57). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to replace the stud bumps disclosed by Wieczorek et al., Nakajyo et al., & Yamamoto et al. with wire, as taught by Doyle et al. since the spacers claimed by Applicant and the spacers used by Wieczorek et al., Nakajyo et al., & Yamamoto et al. are well known alternate types of spacers which will perform the same function, if one is replaced with the other, of creating gaps between dielectric elements.

Response to Arguments

4. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941

(Fed. Cir. 1992). In this case, the knowledge to one of ordinary skill in the art that uniform gap width and strong epoxy films are beneficial to semiconductor devices are sufficient motivation, as disclosed above in paragraph 2.

5. In response to applicant's arguments that the implementation of the adhesives and stud bumpers between the CMOS chip and bond pad on the printed circuit board can not be conclusively asserted to ensure the standard flatness between scintillator and CMOS chip; these arguments have been fully considered but they are not persuasive since the suggestion of standard flatness is inherent to the feature of a layer of stud bumps/spacers, since the stud bumps/spacers are all of a standard size, as detailed above in paragraph 2.

6. In response to applicant's arguments that one side being higher than another does not guarantee a minimal stretch of electrical leads; these arguments have been fully considered but they are not persuasive since the motivation to add spacer is to prevent one side from being higher than the other, as detailed above in paragraph 2.

7. In response to applicant's arguments that Wieczorek does not denounce certain types of adhesive layers nor does Nakajyo disclose that certain types of adhesives and spacers are the best technique for bonding elements; these arguments have been fully considered but they are not persuasive since "best" or "insufficient" are not considered to be the sole reason to combine features of two references; the combination must only be shown to be obvious, as detailed above in paragraph 2. Furthermore, the fact that the references do not explicitly mention stretch effects on the electrical leads of the Wieczorek et al. Nakajyo et al. & Yamamoto et al. devices does not preclude one skilled in the art from recognizing such a feature inherent to such devices as motivation to combine said features of the references.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Travis M. Reis whose telephone number is (571) 272-2249. The examiner can normally be reached on 8--5 M--F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for all communications.

Travis M Reis
Examiner
Art Unit 2859

Diego Gutierrez
Supervisory Patent Examiner
Technology Center 2800

tmr
May 4, 2005

CHRISTOPHER W. FULTON
PRIMARY EXAMINER